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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,140	02/17/2004	William E. Dougherty JR.	YOR920030437US1 (8728-653	9678

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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
DINH, PAUL	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,140	DOUGHERTY ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is a response to amendment filed on 2/20/07.

Claims 1-14 are pending.

Claim Objections

Claims 1, 13 and 14 are objected to because "property" is not clearly described in the disclosure and in claims 1, 13 and 14. See 37 CFR 1.75 (d).

Claims 1, 13 and 14 are objected to because "network graph" is not defined in claims 1, 13-14.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Gupta et al (US Pub. 2004/0068711)

(Claim 1 and similarly recited claims 13-14)

During a logical synthesis stage of a circuit design (*see title, abstract, fig 1-3; digital synthesis = logical synthesis, fig 1 = digital circuit synthesis, etc.*)

Generating a network graph from a logical representation of the circuit design

(The dependence graph in fig. 2 and/or the program graph in steps 102, 104, and fig 3 (Fig. 3 used in step 106) is/are considered as (equivalent to) the claimed network graph

because these dependence/program graphs include property as claimed, and/or include edges, nodes, connections, congestion, paths, distance, etc, as the network graph disclosed in the application specification. Graph from a *logical representation is, i.e., one or more of: digital circuit (title, abstract, fig 1 (digital circuit synthesis), Function specification (fig 1, para. 0024), macrocell library (fig 1), graph includes operations such as additions, multiplications, subtractions (para 0028), latches/functional units in hardware representation (0031), etc.)*

Determining a structural metric from a property of the network graph, *(Structural metric is simply a routability consideration (abstract), circuit performance expression, metric expression, estimation (para 0003), measure, evaluation, prediction, consideration (para 0043, 0048-0049, 0052, 0077, 0087). Property of the network graph is, i.e., one or more of: nodes, edges, connections, interconnections, text based intermediate code, intermediate representation, routability, wires, paths, latency, distance, timing, delay, clock boundary/cycle, schedule, constraints, cost, netlist modeled from program graph, etc.)*

Wherein the structural metric predict congestion characteristics during optimization of the circuit design; and

(Predict/estimate/evaluate congestion characteristics, i.e., see on one or more of: abstract, fig 1, 3, para 0010, 0040, 0041, 0042, 0043, 0049, 0057, 0062, 0063, 0076, 0092, etc; Predict/estimate/evaluate congestion characteristics during optimization of the circuit design are, i.e., see on one or more of: abstract, fig 1, 3 (Predict/estimate/evaluate congestion characteristics during optimizing/improving/synthesizing the circuit design); and para 0040, 0041, 0063, 0064, etc.)

Using the structural metric during the logic synthesis stage to optimize the circuit design *(Title, abstract, field of invention, fig 1, 3 (digital circuit synthesis) and corresponding text, i.e., para 0005-0009, 0021, 0029-0030, 0044, 0048, 0056, 0061, 0064, 0084, 0095, 0095, etc)*

(Claim 2) wherein using the structural metric during the logic synthesis to optimize circuit design model comprises adding, deleting or substituting one or more circuits using a combination of Boolean, algebraic and electrical optimizations (fig 1-3).

(Claim 3) wherein the structural metric includes a measure of routing congestion of the circuit design after placement and routing, the routing congestion being measured by an average and a peak number of wires crossing any bisection of the placed and routed circuit design (one or more of: para 0040-0043, 0049, 0057, 0063-0064, 0076, 0092)

(Claims 4-5) wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the structural metric during a technology independent synthesis stage of the logic synthesis stage (one or more of para 0002, 0021, 0061-

0062, 0096); during the technology mapping stage of the logic synthesis (one or more of para 0002, 0021, 0061-0062, 0096).

(Claim 6) wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the structural metric during a buffering stage of the logic synthesis stage (para 0060, 0072)

(Claim 7) further comprising incrementally updating the structural metric when logic changes are made to the circuit design (one or more of fig 1-3, 6-8, para 0034, 0043-0044, 0056, 0058, 0079-0081).

(Claim 8) wherein incrementally updating the structural metric logic changes are made to the circuit design comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary (one or more of fig 1-3, 6-8, para 0034, 0043-0044, 0056, 0058, 0079-0081).

(Claim 9) wherein incrementally updating the structural metric when logic changes are made to the circuit design comprises performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073).

(Claim 10) wherein creating the structural metric comprises any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), expansion metric (one or more of para 0024, 0033, 0050-0054, fig 2)

(Claim 11) wherein determining a structural metric comprises: generating one or more possible optimizations (this invention about generating one or more possible optimizations i.e., cost, components, power, area, delay, reduction/minimizing manual work, cut, net, congestion, hardware, distance, wire lengths, etc.); incrementally updating the structural metric when the optimizations are made to the circuit design to evaluate the cost of applying each of the one or more possible optimizations to the circuit design (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073), the structural metric comprising any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric (one ore more of para 0024, 0033, 0050-0054); evaluating a structural metric cost of each of the one or more possible optimizations as given by the structural metric (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073); selecting an optimization from the one or more possible optimizations

with the lowest structural metric cost (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073); and applying the optimization to the circuit design (one or more of para 0035, 0037, 0039, 0046-0047, 0055, 0072-0073)

Claims 1 and similarly recited claims 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Cronquist (US pub. 2004/0068331)

During a logical synthesis stage of a circuit design (*see title, this prior art synthesize digital/logic circuit, not analog circuit*)

Generating a network graph from a logical representation of the circuit design

(Program graphs in fig 6-7, 9B considered as (equivalent to) the claimed network graph because these program graphs include property as claimed and/or include edges, nodes, connections, congestion, paths, distance, etc, as the network graph disclosed in the application specification. Graph from a *logical representation is, i.e., one or more of: digital circuits, Function specification, macrocell library, graph includes operations such as additions, multiplications, subtractions, latches/functional units in hardware representation, etc.)*

Determining a structural metric from a property of the network graph,
(Structural metric is simply a routability consideration, circuit performance expression, metric expression, estimation, measure, evaluation, and prediction consideration. Property of the network graph is, i.e., one or more of: nodes, edges, connections, interconnections, text based intermediate code, intermediate representation, routability, wires, paths, latency, distance, timing, delay, clock boundary/cycle, schedule, constraints, cost, netlist modeled from program graph, etc.)

Wherein the structural metric predict congestion characteristics during optimization of the circuit design (*one or more of: title, abstract, field of invention, para 0011-0013, 0015, 0019, 0020-0022, 0032-0034, 0063, 0071. This prior art about* structural metric (see above-mention structural metric) *predict congestion characteristics during optimization of the circuit design*); and

Using the structural metric during the logic synthesis stage to optimize the circuit design
(One or more of: title, para 0003, 0005, 0012, 0032-0035, 0039, 0047, 0062, 0067; this prior art about using the structural metric (see above-mention structural metric) during the logic synthesis stage to optimize the circuit design)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Primary Examiner